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(56) Documents Cited
GB 2199182 A GB 1195301 A EP 0645953 A1
WO 95/03683 A1 US 4993148 A

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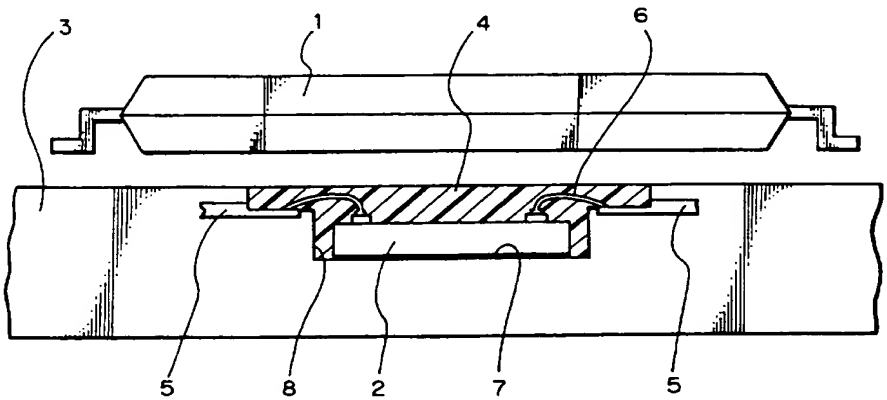
(54) **Mounting semiconductor devices in stepped recesses in a circuit board**

(57) In a multi-chip module, a laminated wiring board (3) is formed with stepped recesses (8). Electrodes (5) to be connected to the electrodes of a bare-chip semiconductor device are subjected to non-electrolytic gold plating. This realizes wire bonding which is as short in distance and as low in loop as possible. To seal each recess with insulating resin, use is made of screen printing using a mesh screen which has a great aperture ratio and a small thickness. In a further embodiment, (Fig 3, not shown), a stepped through hole is formed in the circuit board, in which the device is mounted using vacuum suction.

Fig. 1



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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

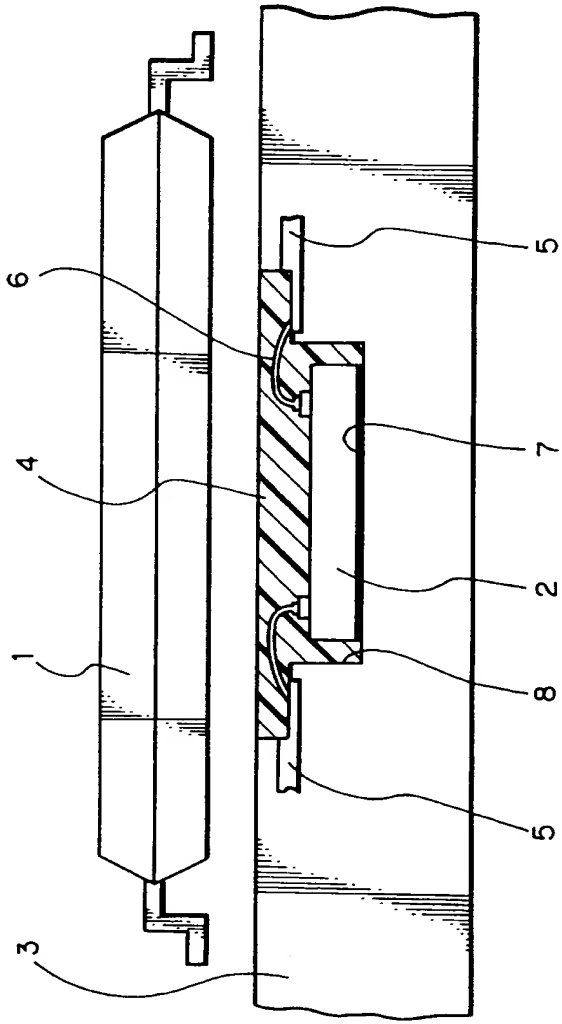


Fig. 1

Fig. 2

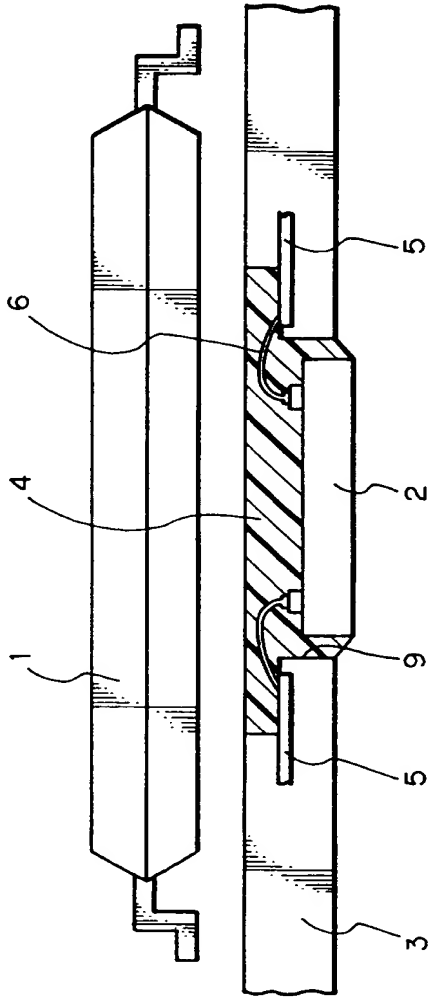
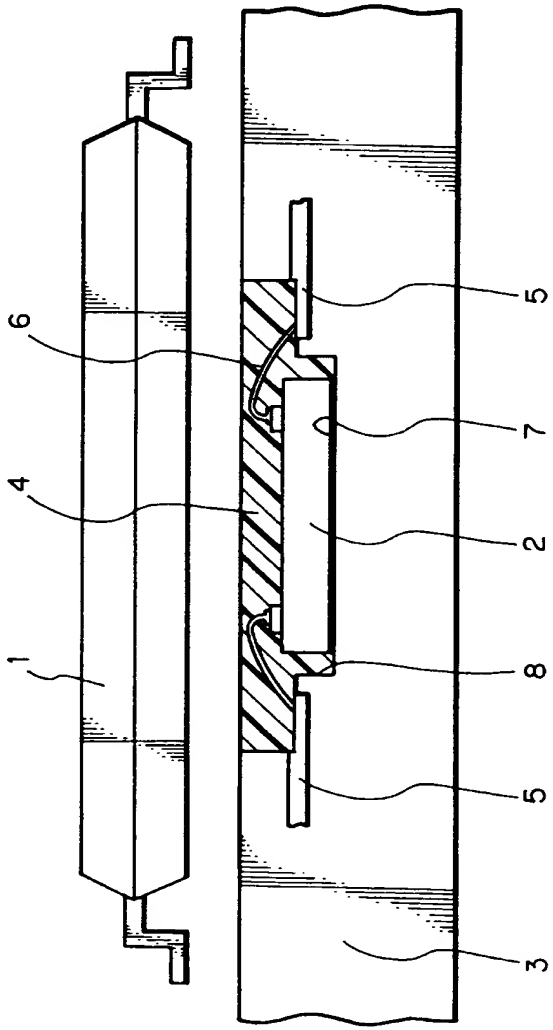


Fig. 3



SEMICONDUCTOR DEVICE MOUNTING METHOD AND MULTI-CHIP MODULE PRODUCED BY THE SAME

The present invention relates to a method of mounting a semiconductor device, and a multi-chip module produced by the same.

A laminate wiring board formed with recesses has been proposed in various forms in the past. For example, Japanese Patent Laid-Open Publication No. 64-57653 teaches a laminate wiring board formed with recesses such that the electrodes of each part and the conductor pattern of the wiring board are flush with each other. This kind of configuration minimizes the distance of connection and is adapted for composite IC (Integrated Circuit) parts.

Japanese Patent Laid-Open Publication No. 1-258446 discloses a laminate thick film wiring board formed with recesses for receiving chips. This kind of configuration is adapted for composite ICs.

Japanese Patent Laid-Open Publication No. 4-359462 discloses a composite IC device formed with recesses in order to protect semiconductor devices from contamination

and deterioration due to flux. The recesses are sealed with sealing members.

Japanese Patent Laid-Open Publication No. 7-30059 proposes a multi-chip module having semiconductor devices mounted in the recesses of a laminate wiring board, and packaged semiconductor devices each being mounted over the respective semiconductor device. With this configuration, it is possible to implement a dense and miniature multi-chip module. The recesses and bare-chip semiconductor devices buried in the recesses promote high integration and miniaturization because the area of the wiring board is determined by the area and number of surface mounting parts as represented by packaged semiconductor devices. However, this document does not show or describe how it produces such a module or how it reduces the thickness of the module specifically.

The conventional laminate wiring boards of the kind described above have the following problems left unsolved. The recesses are formed in the wiring board in order to reduce the mounting area, and the bare-chip semiconductor devices are received in the recesses. The prerequisite with this scheme is that resin sealing the recesses should be prevented from protruding from the top of the wiring board. This requires the recesses to have a substantial depth and thereby obstructs the reduction of the thickness of the wiring board.

Furthermore, to allow each packaged semiconductor device to be mounted while straddling the respective recess, it is necessary to reduce the area of each recess.

It is therefore an object of at least the preferred embodiments of the present invention to provide a highly integrated, thin and light weight multi-chip module, and a method of mounting a semiconductor device for producing such a module.

A first aspect of the present invention provides a method of mounting a semiconductor device on a laminate wiring board, comprising the steps of:

(a) forming a recess or a through hole in said laminate wiring board, said recess or said through hole being formed with a stepped configuration;

(b) mounting said device in said recess or through hole;

(c) performing wire bonding of said device to said wiring board; and

(d) sealing said recess or said through hole with sealing resin.

In a preferred embodiment of the first aspect of the present invention, a method of mounting a semiconductor device on a laminate wiring board has the steps of (a) forming a recess or a through hole in the laminate wiring board, and (b) sealing the recess or the through hole with sealing resin. The step (b) has the steps of (c) providing the recess or the through hole with a stepped configuration, and performing screen printing using a mesh screen having a relatively great aperture ratio and a relatively small thickness, and (d) performing wire bonding as short in distance and as low in loop as possible.

A second aspect of the present invention provides a multi-chip module comprising:

a plurality of semiconductor devices; and

a laminate wiring board;

wherein said laminate wiring board has a plurality of recesses or through holes having a stepped configuration, and wherein each of said plurality of semiconductor devices is mounted in a respective recess or through hole and sealed therein.

A third aspect of the present invention provides a multi chip module comprising:

a plurality of surface mounting parts;

a plurality of bare-chip semiconductor devices; and

a laminate wiring board;

wherein said wiring board has a plurality of recesses or through holes, and wherein each of said plurality of semiconductor devices is mounted in a respective recess or through hole and sealed therein.

In a preferred embodiment of the third aspect of the present invention, a multi-chip module has a plurality of surface mounting parts as represented by packaged semiconductor devices, a plurality of bare-chip semiconductor devices, and a laminate wiring board. The laminate wiring board is formed with a plurality of recesses. The plurality of bare-chip semiconductor devices are each mounted in the respective recess and sealed by resin.

In another preferred embodiment of the third aspect of the present invention, a multi-chip module has a plurality of surface mounting parts as represented by packaged semiconductor devices, a plurality of bare-chip semiconductor devices, and a laminate wiring board. The wiring board is formed with a plurality of through holes. The plurality of bare chips are each mounted in the respective recess and sealed therein.

Preferred features of the present invention will now be described, purely by way of example only, with reference to the accompanying drawings, in which:-

FIG. 1 is a vertical section showing a multi-chip module embodying the present invention;

FIG. 2 is a vertical section showing an alternative embodiment of the present invention; and

FIG. 3 is a vertical section showing another alternative embodiment of the present invention.

Referring to FIG. 1 of the drawings, a multi-chip module embodying the present invention is shown. In FIG. 1, a

packaged semiconductor device 1 is shown as being spaced above a laminate wiring board 3 in a particular assembly stage. The wiring board 3 is formed with a plurality of stepped recesses 8 (only one is shown). The stepped recesses 8 each has a lower layer and an upper layer. A bare-chip semiconductor device 2 is affixed to the wiring board 3 by adhesive 7 in the lower layer of each recess 8. Electrodes 5 provided on the upper layer of the recess 8 of the wiring board 3 are connected to the electrodes of the semiconductor device 2.

The electrodes 5 of the wiring board 3 are subjected to non-electrolytic gold plating for the following reasons. Electrolytic plating would cause the electrodes 5 to protrude from the side walls of the recess 8 and might cause them to contact the side edges of the semiconductor device 2, resulting in short-circuiting. If sufficient distances were provided between the side walls of the recess 8 and those of the semiconductor device 2 in order to avoid the above short-circuiting, the area of the recess 8 would be undesirably increased.

The method by which this preferred embodiment of the present invention mounts the semiconductor devices 1 and 2 will be described with reference to FIG. 1. First, the bare-chip semiconductor device 2 is mounted in the lower layer of the recess 8. Then, the electrodes of the semiconductor device 2 and the electrodes 5 of the wiring

board 3 are connected together by wire bonding using gold, copper or aluminum wires 6.

The semiconductor device 2 mounted in the recess 8 is sealed by insulating resin 4. For example, assume that the packaged semiconductor device 1 is a TSOP or a TQFP package whose mounting height is limited to 1.27 mm. Then, the distance between the bottom of the semiconductor device 1 and the top of the wiring board 3 is limited to 0.05 $\pm$ 0.05 mm. In this condition, it is quite likely that the bottom of the semiconductor device 1 contacts the top of the wiring board 3.

If the insulating resin 4 sealing the recess 8 protrudes from the top of the wiring board 3, it will contact the bottom of the semiconductor device 1 and will thereby raise leads away from lands provided on the wiring board 3, resulting in defective soldering. In light of this, the illustrative embodiment uses screen printing for the purpose of feeding the resin 4 in a preselected constant amount. To promote the smooth delivery of the resin 4, use is made of a screen mesh having a large aperture ratio. The mesh screen should preferably be as thin as possible in order to realize a sealing height of less than 50 μm.

To effectively use the wiring board 3, the packaged semiconductor device 1 or similar comparatively large sized part is mounted on the wiring board 3 in such a manner as to

straddle the recess 8. In this sense, the area of the recess 8 should preferably be small, as stated earlier. Because the area of the recess 8 cannot be decreased below the area of the semiconductor device 2, implementing short distance, low loop bonding is important. In the illustrative embodiment, the layer of the wiring board 3 in which the electrodes 5 are formed is positioned about 10 μm higher in level than the electrode plane of the semiconductor device 2. This successfully reduces the distance of connection.

FIG. 3 shows a second embodiment of the present invention. As shown, with the state-of-the-art bonding technologies, lower loop bonding is achievable when the electrode plane of the semiconductor device 2 is increased in height. The rest of the configuration is identical with the embodiment shown in FIG. 1.

FIG. 2 shows another alternative embodiment of the present invention similar to the foregoing embodiments except for the following. As shown, when the laminate wiring board 3 is too thin to form the stepped recess, the stepped recess is replaced with a through hole 9. In this embodiment, the adhesive 7 of the previous embodiments is replaced with vacuum suction. Specifically, to affix the semiconductor device 2 to the wiring board 3, the device is sucked from below. The rest of the configuration is identical with the embodiment shown in FIG. 1.

In summary, in accordance with the present invention, a laminate wiring board is formed with stepped recesses. Electrodes to be connected to the electrodes of a bare-chip semiconductor device are subjected to non-electrolytic gold plating. This realizes wire bonding which is as short in distance and as low in loop as possible. To seal each recess with insulating resin, use is made of the screen printing using a mesh screen which has a large aperture ratio and a small thickness. Therefore, each recess can have its depth and size respectively limited to about +200 μm and about +4 mm which are the thickness and size of the chip. That is, dimensions for mounting a packaged semiconductor device, which is one of surface mounting parts occupying comparatively broad areas, in a laminated wiring board as a bare-chip semiconductor device can be defined. As a result, the laminate wiring board is reduced in size and thickness.

It will be understood that the present invention has been described above purely by way of example, and modifications of detail can be made within the scope of the invention.

Each feature disclosed in the description, and (where appropriate) the claims and drawings may be provided independently or in any appropriate combination.

CLAIMS

1. A method of mounting a semiconductor device on a laminate wiring board, comprising the steps of:

(a) forming a recess or a through hole in said laminate wiring board, said recess or said through hole being formed with a stepped configuration;

(b) mounting said device in said recess or through hole;

(c) performing wire bonding of said device to said wiring board; and

(d) sealing said recess or said through hole with sealing resin.

2. A method according to Claim 1, wherein said recess or through hole is sealed using a screen printing technique employing a mesh screen.

3. A method according to Claim 1 or Claim 2, wherein electrodes are formed on said wiring board using a non-electrolytic gold plating technique.

4. A method according to Claim 3, wherein said stepped recess or through hole comprises a relatively wider portion and a relatively narrower portion, said electrodes being formed in said relatively wider portion.

5. A method according to Claim 4, wherein said electrodes are spaced from the side walls of said relatively narrower portion of said recess or through hole.

6. A method according to any of Claims 2 to 5, wherein the mesh screen has a relatively large aperture ratio and a relatively small thickness.

7. A method according to any of the preceding claims, wherein said stepped recess or through hole comprises a relatively wider portion and a relatively narrower portion, and said relatively narrower portion is formed with a depth greater than a thickness of said semiconductor device.

8. A multi-chip module comprising:

a plurality of semiconductor devices; and

a laminate wiring board;

wherein said laminate wiring board has a plurality of recesses or through holes having a stepped configuration, and wherein each of said plurality of semiconductor devices is mounted in a respective recess or through hole and sealed therein.

9. A multi-chip module according to Claim 8, wherein each of said plurality of stepped recesses or through holes comprises a relatively wider portion and a relatively narrower portion, said relatively narrower portion having a depth greater than a thickness of said semiconductor device.

10. A multi-chip module according to Claim 8 or Claim 9, wherein each of said plurality of stepped recesses or through holes comprises a relatively wider portion and a relatively narrower portion, and said module further comprises electrodes disposed in said relatively wider portion of each of said plurality of recesses or through holes.

11. A multi-chip module according to Claim 10, wherein said electrodes are spaced from the side walls of said relatively narrow portion.

12. A multi-chip module according to any of Claims 8 to 11, further comprising a plurality of devices mounted on the surface of said module.

13. A multi-chip module according to any of Claims 8 to 12, wherein said recesses or though holes are sealed with resin.

14. A multi-chip module comprising

a plurality of surface mounting parts;

a plurality of bare-chip semiconductor devices; and

a laminate wiring board;

wherein said wiring board has a plurality of recesses or through holes, and wherein each of said plurality of semiconductor devices is mounted in a respective recess or through hole and sealed therein.

15. A module according to Claim 14, wherein each of said recesses or through holes has a stepped configuration, each of said plurality of stepped recesses or through holes comprising a relatively wider portion and a relatively narrower portion, said relatively narrower portion having a depth greater than a thickness of said semiconductor device.

16. A method of mounting a semiconductor device on a laminate wiring board substantially as herein described with reference to the accompanying drawings.

17. A multi-chip module substantially as herein described with reference to and as shown in the accompanying drawings.

The Patent Office

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Application No: GB 9612613.1 **Examiner:** Steven Davies
Claims searched: 3-1 **Date of search:** 3 October 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1R-RAA,RAB,RAR,RBJ

Int Cl (Ed.6): H05K-1/00,1/18

Other: Online WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2199182 A	(MARCONI) the whole document	8-11
Y	GB 1195301	(FORMICA) e.g. page 2, lines 37-43; page 3, lines 69-90	2,6
X,Y	EP 0645953 A1	(SIEMENS) e.g. Fig.9	X:1,4,5,7-11,13 Y:2,3,6,12
Y	WO 95/03683 A1	(OAKLEIGH SYSTEMS) page 10,last para.-page 13,line 5	12
Y	US 4993148	(MITSUBISHI) e.g.col.5,line 65-col.6,line 46	3

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

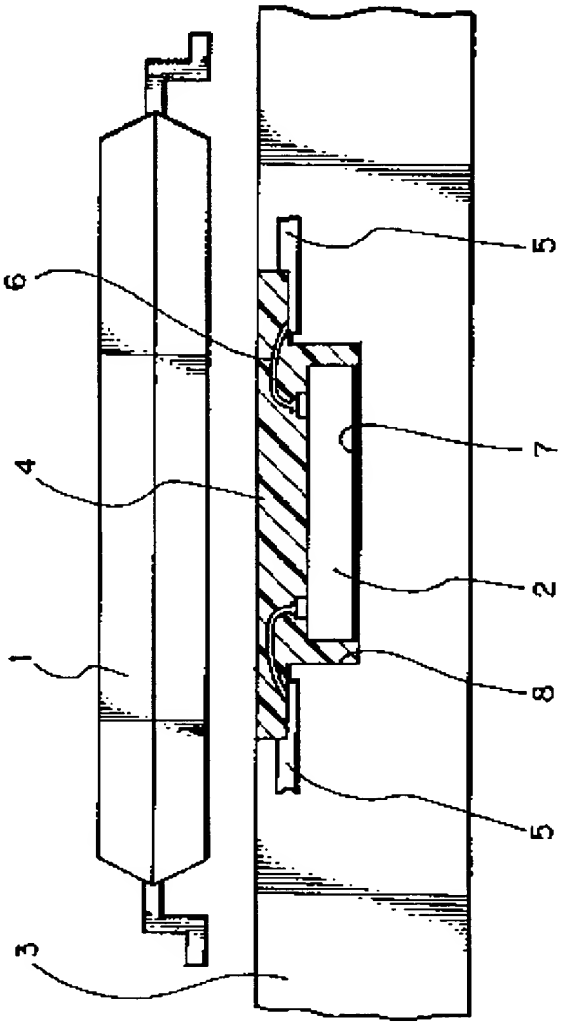
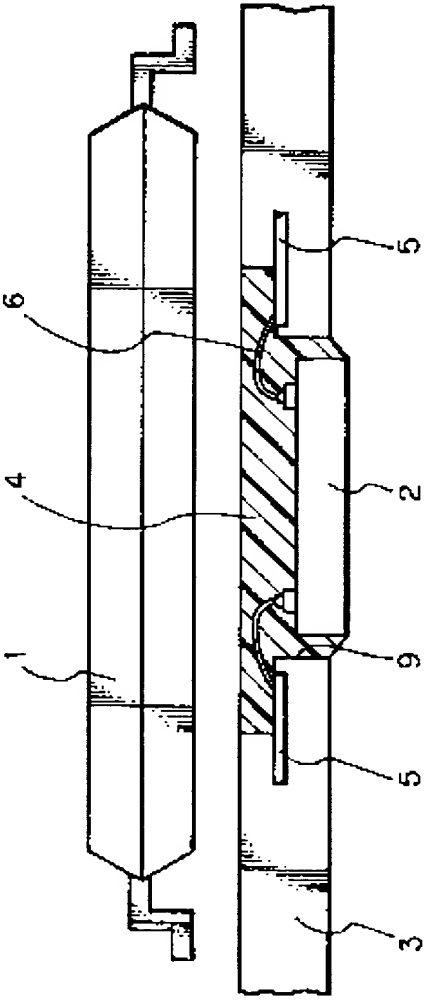


Fig. 1

Fig. 2



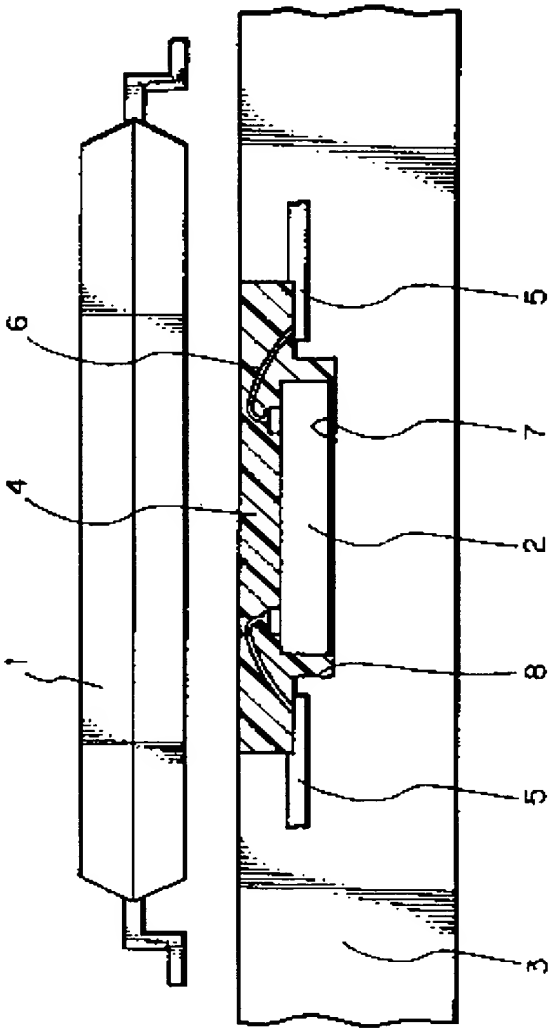


Fig. 3